49. A floating gate transistor structure, comprising:

a substrate comprising semiconductive material;

a pair of spaced shallow trench isolation (STI) masses received within and projecting outwardly from the semiconductive material, the masses having opposing sides defining a region therebetween over the semiconductive material and an active area therebetween within the semiconductive material;

a floating gate received within the region and over the active area; and

a control gate operatively over the floating gate.

50. The floating gate transistor of Claim 49, where the floating gate only partially fills the region.

51. The floating gate transistor of Claim 49, where the floating gate completely fills the region.

52. The floating gate transistor of Claim 49, where the floating gate comprises a roughened uppermost surface.

53. The floating gate transistor of Claim 49, where the floating gate only partially fills the region and comprises an essentially concave uppermost surface.

54. The floating gate transistor of Claim 49, where the floating gate comprises hemispherical grain polysilicon.

55. The floating gate transistor of Claim 49, where the active area has a first cross-sectional dimension and the region has a second cross-sectional dimension, the first cross-sectional dimension being parallel to and smaller than to the second cross-sectional dimension.

56. The floating gate transistor of Claim 55, where the floating gate only partially fills the region and comprises an essentially concave uppermost surface.

57. The floating gate transistor of Claim 55, where the floating gate comprises a roughened uppermost surface.

58. The floating gate transistor of Claim 49, where the active area has a first cross-sectional dimension and the region has a second cross-sectional dimension, the first cross-sectional dimension being parallel to and essentially equal to the second cross-sectional dimension.

59. The floating gate transistor of Claim 58, where the floating gate only partially fills the region and comprises an essentially concave uppermost surface.

60. The floating gate transistor of Claim 59, where the essentially concave uppermost surface is roughened.

61. (Amended) A floating gate transistor structure, comprising:

a substrate comprising semiconductive material;

a pair of spaced shallow trench isolation (STI) masses having first portions received within the semiconductive material and second portions projecting outwardly from the semiconductive material, the first and second portions each having opposing sides, the opposing sides of the first portions defining an active area therebetween having a first cross-sectional dimension and the opposing sides of the second portions defining a region therebetween having a second cross-sectional dimension;

a first dielectric layer received within the region and overlying the active area;

a floating gate received within the region and overlying the first dielectric layer;

a second dielectric layer overlying the floating gate; and

a control gate operatively overlying the second dielectric layer and operatively coupled to the floating gate.

62. The floating gate transistor of Claim 61, where the second cross-sectional dimension is larger than the first cross-sectional dimension.

63. The floating gate transistor of Claim 61, where the floating gate only partially fills the region and comprises an essentially concave uppermost surface.

64. The floating gate transistor of Claim 63, where the floating gate comprises hemispherical grain polysilicon.

65. The floating gate transistor of Claim 61, where the floating gate completely fills the region and comprises a rugged outermost surface.

66. The floating gate transistor of Claim 61, where the second cross-sectional dimension is essentially equal to the first cross-sectional dimension.

67. The floating gate transistor of Claim 66, where the floating gate comprises hemispherical grain polysilicon, only partially fills the region and has an essentially concave uppermost surface.

68. The floating gate transistor of Claim 66, where the floating gate completely fills the region.

69. The floating gate transistor of Claim 68, where the floating gate comprises a rugged outermost surface.